CLAIMS

1. A reconfigurable processor comprising:

a substrate;

a plurality of nodes disposed on said substrate; and

at least one plurality of circuits disposed on said substrate, each of said circuits being operatively connected, and thereby clustered, with respect to a first of said switching nodes.

2. The invention of Claim 1 further including addressing means for selectively addressing said circuits.

3. The invention of Claim 1 wherein said at least one node is a crossbar switch.

4. The invention of Claim 3 wherein said crossbar switch is an arithmetic crossbar switch.

5. The invention of Claim 4 wherein at least one of said circuits is an arithmetic logic unit.

6. The invention of Claim 5 wherein plural of said circuits are arithmetic logic units.

7. The invention of Claim 1 wherein at least one of said nodes is a memory node.

8. The invention of Claim 7 further including plural memories operatively connected to said memory node.

9. A reconfigurable processor comprising:

a substrate;

a plurality of arithmetic clusters disposed on said substrate, each of said arithmetic clusters including an arithmetic crossbar switch and a plurality of processing elements connected thereto;

a plurality of memory clusters disposed on said substrate, said memory clusters interconnecting said arithmetic clusters and each of said memory clusters including a memory crossbar switch and a plurality of memory elements connected thereto; and

means for selectively addressing said clusters and said elements connected thereto.

10. The invention of Claim 9 wherein at least one of said processing elements is an arithmetic logic unit.

11. The invention of Claim 10 wherein plural of said processing elements are arithmetic logic units.

12. The invention of Claim 9 wherein at least one of said processing elements is a multiplier/accumulator.

13. The invention of Claim 12 wherein plural of said processing elements are multiplier accumulators.

14. The invention of Claim 9 wherein said means for selectively addressing said clusters and said elements includes a switch configuration register.

15. The invention of Claim 9 wherein said means for selectively addressing said clusters and said elements includes an element configuration register.

16. A method for processing data including the steps of:

configuring a reconfigurable processor including:

a substrate,

a plurality of switching nodes disposed on said substrate, and

at least one plurality of circuits disposed on said substrate, each of said circuits being operatively connected, and thereby clustered, with respect to a first of said switching nodes;

selectively activating selective ones of said nodes; and

selectively communicating data to at least one of said circuits connected to said selective ones of said nodes.